

Contents

Executive Summary	I
Zusammenfassung	III
1 Introduction	1
1.1 Background	1
1.2 State of the Art	2
1.3 Problem	3
1.4 Scope of the Work	4
1.5 Research Questions	6
1.6 Structure of the Thesis	7
2 Substrate-Related Switching Characteristics of GaN-on-Si Half-Bridges	9
2.1 Problem and Approach	9
2.2 Capacitances of Individual Transistors	11
2.2.1 Terminal Capacitances of Three- and Four-Terminal HEMTs	11
2.2.2 Effective Capacitances	12
2.2.3 Non-linear Multi-Bias Capacitances	13
2.2.4 Condensed Capacitances-Related Quantities at Nominal Operation Voltage	15
2.3 Limited Operation Voltage from Substrate Biasing	16
2.4 Analyzed Half-Bridge Substrate Terminations	19
2.5 Substrate Voltage Analysis	20
2.5.1 Substrate-to-Source Voltage Calculation for Fixed Substrate Terminations	20
2.5.2 Substrate-to-Source Voltage Calculation for Floating Substrate Terminations	22
2.5.2.1 Separately Floating Substrate Terminations	22
2.5.2.2 Common Floating Substrate Termination	24
2.5.3 Transient Substrate Voltage Extrema and Swing	25
2.5.4 Semi-Floating Substrate Termination Networks	26
2.5.5 Calculation of Substrate Voltages using Measured Capacitance Data	29
2.6 Capacitance Transformation for Half-Bridges to Eliminate Substrate Dependence	30
2.6.1 Method for Half-Bridges Without and With Coupled Substrates	32
2.6.2 B=S (conventional) Termination	34
2.6.3 B=D Termination	35
2.6.4 B=G Termination	36

2.6.5	Separately B-Floating Termination (Discrete Devices)	36
2.6.6	Common B-Floating Termination (Half-Bridge)	37
2.7	Calculated Switching Characteristics for Different Substrate Terminations	38
2.7.1	Output-Related Effective Capacitances $C_{\text{oss}}, C_{\text{sw}}, C_{\text{dc}}$	38
2.7.2	Switching Energies E_{oss} and E_{qoss}	41
2.7.3	Switching Charges Q_{oss} and Q_{sw}	41
2.7.4	Feedback-Related Effective Capacitances $C_{\text{rss}}, C_{\text{xss}}$	42
2.7.5	Input-Related Effective Capacitances $C_{\text{iss}}, C_{\text{rss}}, C_{\text{xss}}$	43
2.8	Experimental Switching Characteristics for Different Substrate Terminations	45
2.8.1	Experimental Setup for Substrate Termination Variation	45
2.8.2	Switching Energies E_{sw}	46
2.8.3	Switch-Node Charge Q_{sw}	47
2.8.4	Reverse Feedback-Related Quantities	48
2.8.5	Resistance Increase for Different Substrate Terminations	50
2.8.6	Dc-Dc Converter Efficiency for Different Substrate Terminations	51
2.8.7	Duty-Cycle Dependent Power Loss	52
2.8.8	Verification of Duty-Cycle Independent Substrate Biasing Network	53
2.9	Experimental Monolithic GaN-on-Si Half-Bridge and Driver Operation	56
2.10	Summary and Conclusion	57
3	Low-Inductive and Clean Switching of Half-Bridges and Gate Drivers	61
3.1	Problem and Approach	61
3.2	Analysis of Parasitic Inductance-Related Voltage Switching Transitions	63
3.2.1	Instantaneous Step-Voltage Switching	63
3.2.2	Limited Voltage Slew-Rate Switching	69
3.2.3	Discrepancy between Measured and Intrinsic Switching Times	75
3.3	Experimental Overshoot Measurement for Limited Slew-Rate Switching	77
3.4	Estimation of Typical Damping Factors and Optimal Switching Times	80
3.5	Reduction of Parasitic Gate-Loop and Power-Loop Inductance	81
3.5.1	Monolithic Integrated Gate Driver	81
3.5.2	Monolithic Integrated Half-Bridge	86
3.5.3	Package-Level Integration using PCB-Embedding	90
3.5.4	Quantified Reduction of the Parasitic Inductance	90
3.5.5	Discussion of Low-Inductive Integration Approaches	92
3.6	Experimental PCB-Embedded Discrete Half-Bridge with Drivers and On-package Capacitors	94
3.7	Summary and Conclusion	95
4	Parasitic Substrate-Loop Inductance and Related Instabilities	99
4.1	Problem and Approach	99
4.2	Parasitic Inductance from the Substrate Termination	100
4.3	Equivalent Feedback Amplifier	102
4.3.1	Circuit Transformation Method	102
4.3.2	Full Equivalent Circuit Transformation	103

4.4	Stability Analysis	105
4.4.1	Evaluation of Stability Condition	105
4.4.2	Parameters for Quantitative Stability Evaluation	106
4.4.3	Effect of Gate-Loop and Power-Loop Parasitic Inductance	106
4.4.4	Instabilities from Substrate-Loop Despite Ideal Gate and Power-Loop	108
4.4.5	Parasitic Common-Source Substrate Inductance L_{CSB}	110
4.5	Resistive Damping of Parasitic Substrate-Loop	112
4.6	Experimental Verification of Substrate-Loop Damping Method	113
4.7	Reduction and Avoidance of Parasitic Substrate-Loop Inductance	116
4.8	Summary and Conclusion	118
5	Summary and Conclusion	121
A	Appendix	125
A.1	Star-to-Delta and Star-to-Mesh Transformation	125
A.2	Extraction of Parameters from Measurement Data	126
A.3	Four-Terminal Capacitance Multi-Bias Measurement Data	127
Bibliography		131
Acknowledgment		141